

# MS-7803 Ver: 10 m-ATX : 190 \* 180 mm

## CPU:

INTEL - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH(H61)

## OnBoard Chipset:

HD Audio Codec:Realtek ALC662

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71808A

Flash ROM: 32Mb SPI (PCH)

## Main Memory:

DDRIII (1066/1333MHz) \* 2 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 1

## PWM:

Controller:VRD12 Intersil/ISL6363CRZ 3+1 PHASE

CPU MOSFET Driver: ISL6612ACBZT

CPU VTT: ON NCP5217

CPU SA : OP+MOS

DDR: uP1513

PCH: APL5611CI

## ACPI:

UPI

## Other:

SATA2.0 x3 (PCH)

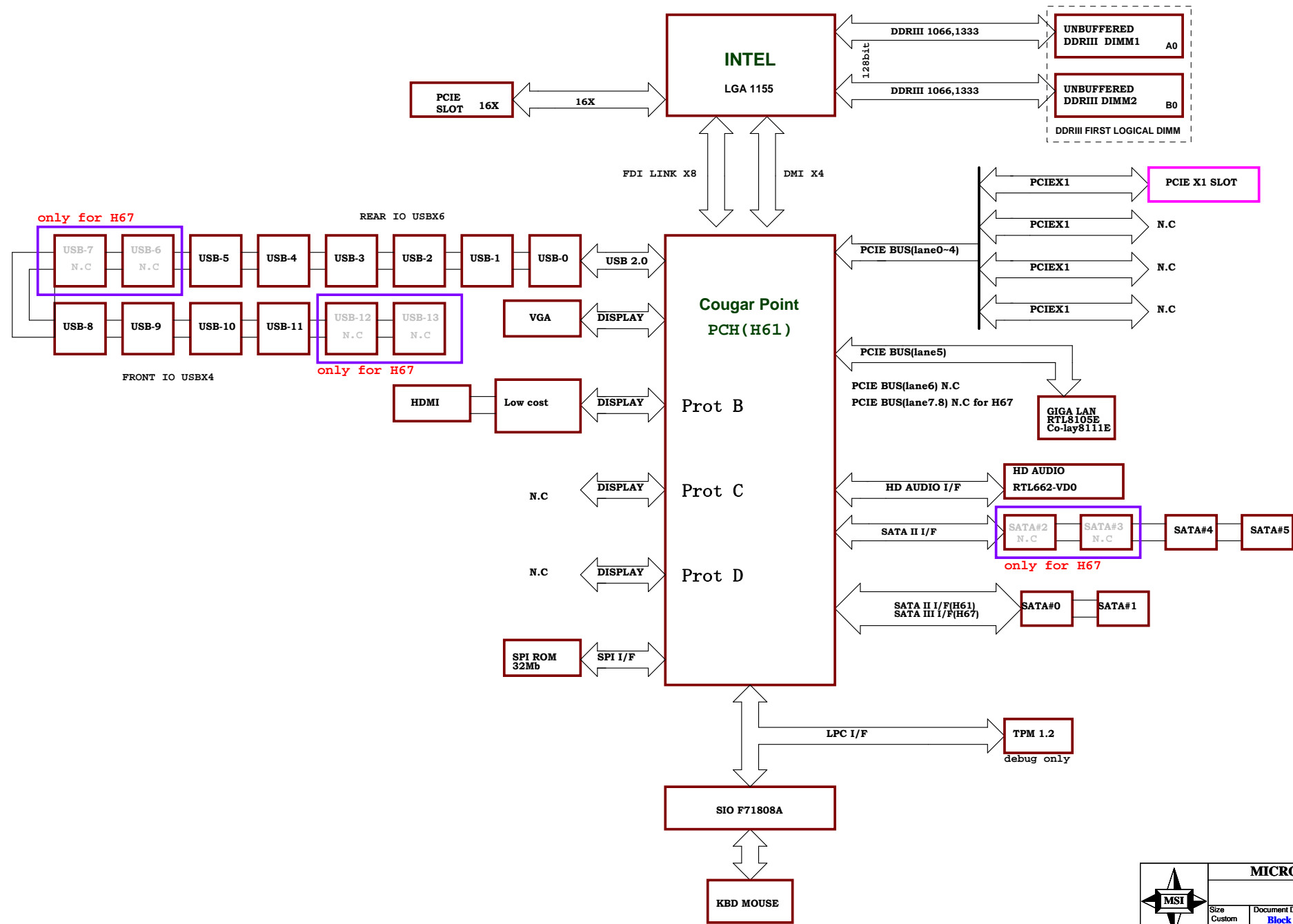
USB2.0 RearX6 Front x4

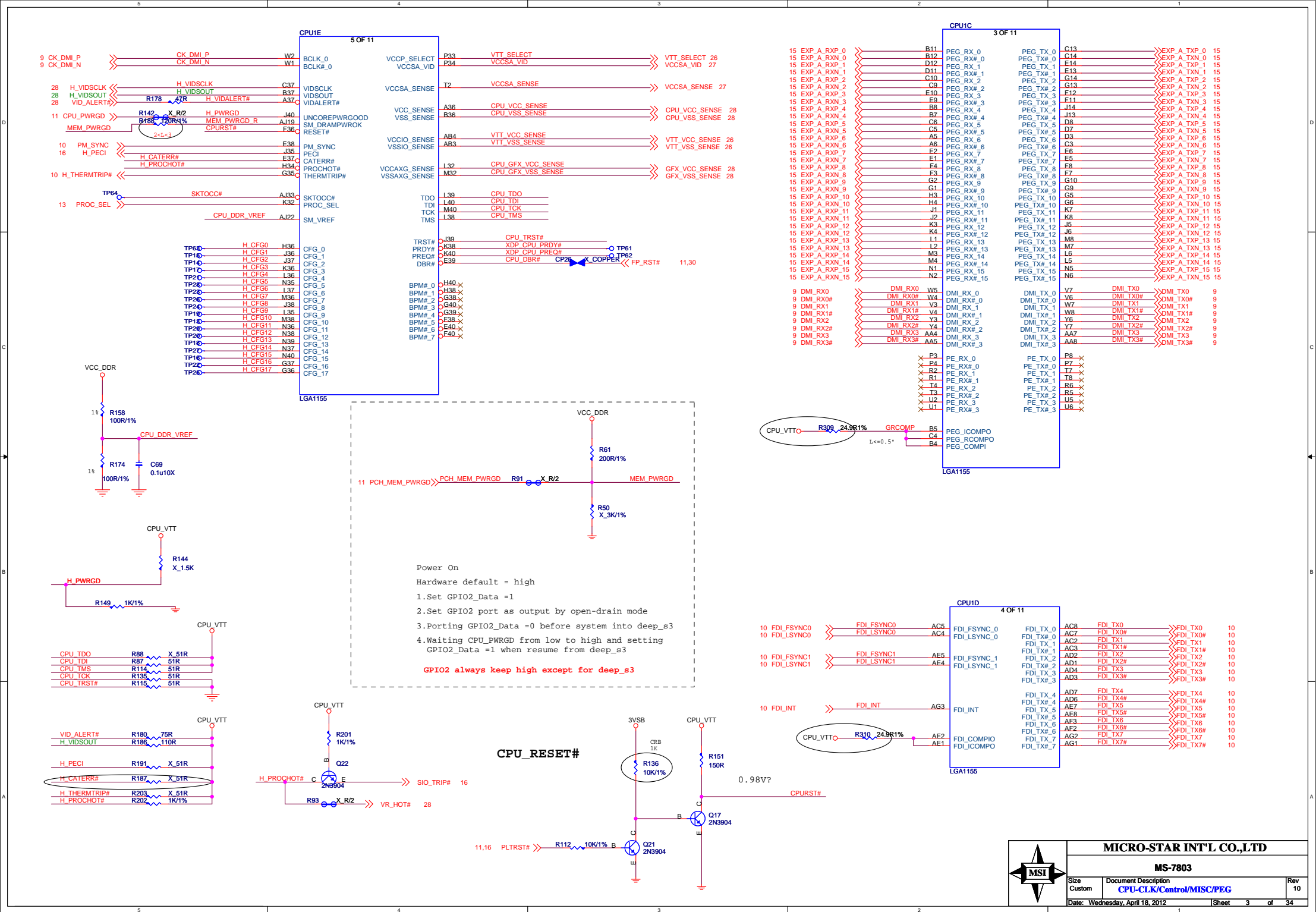
D-SUB/HDMI\*1

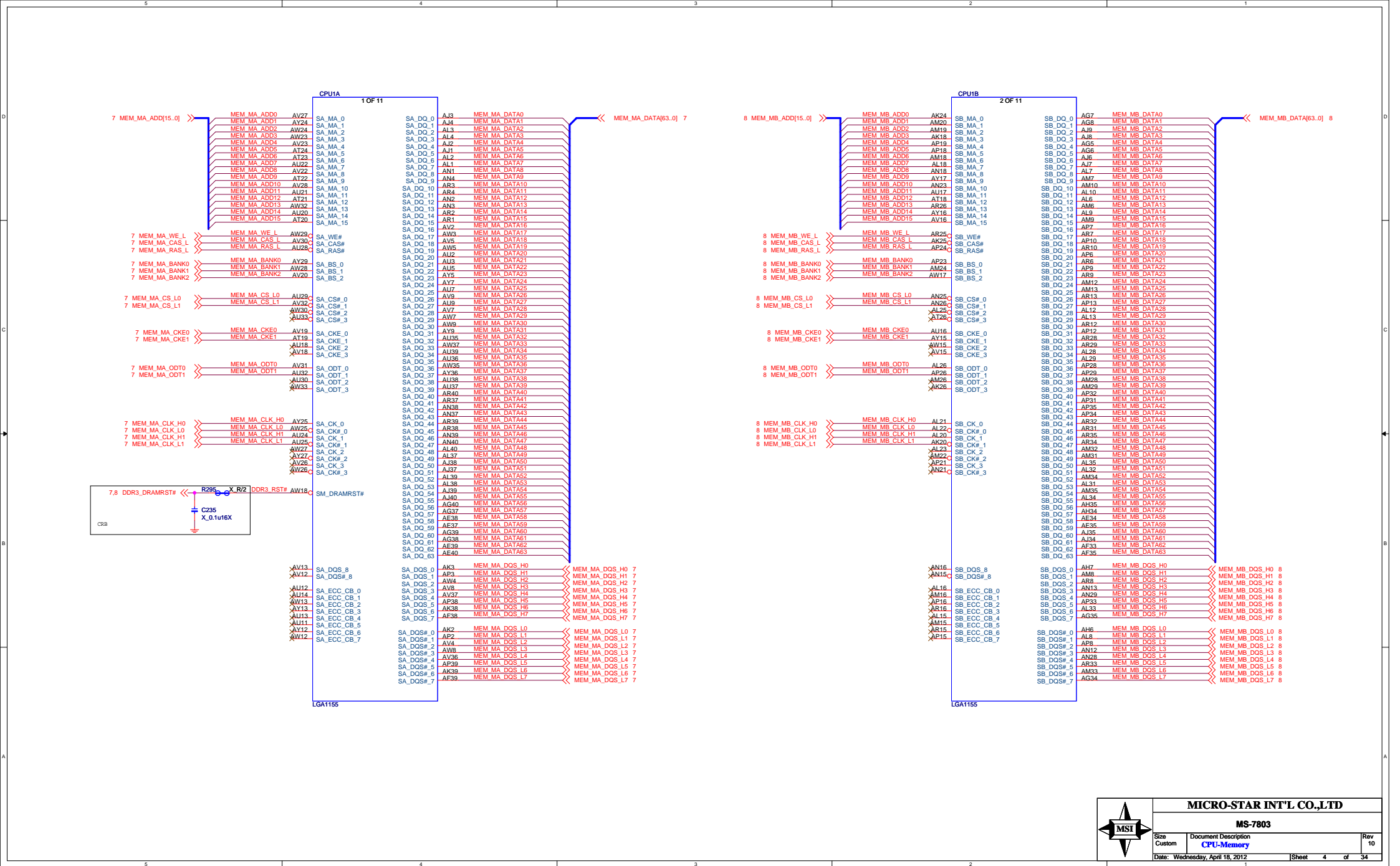
LPC Header \*1

on BOARD BUZZER

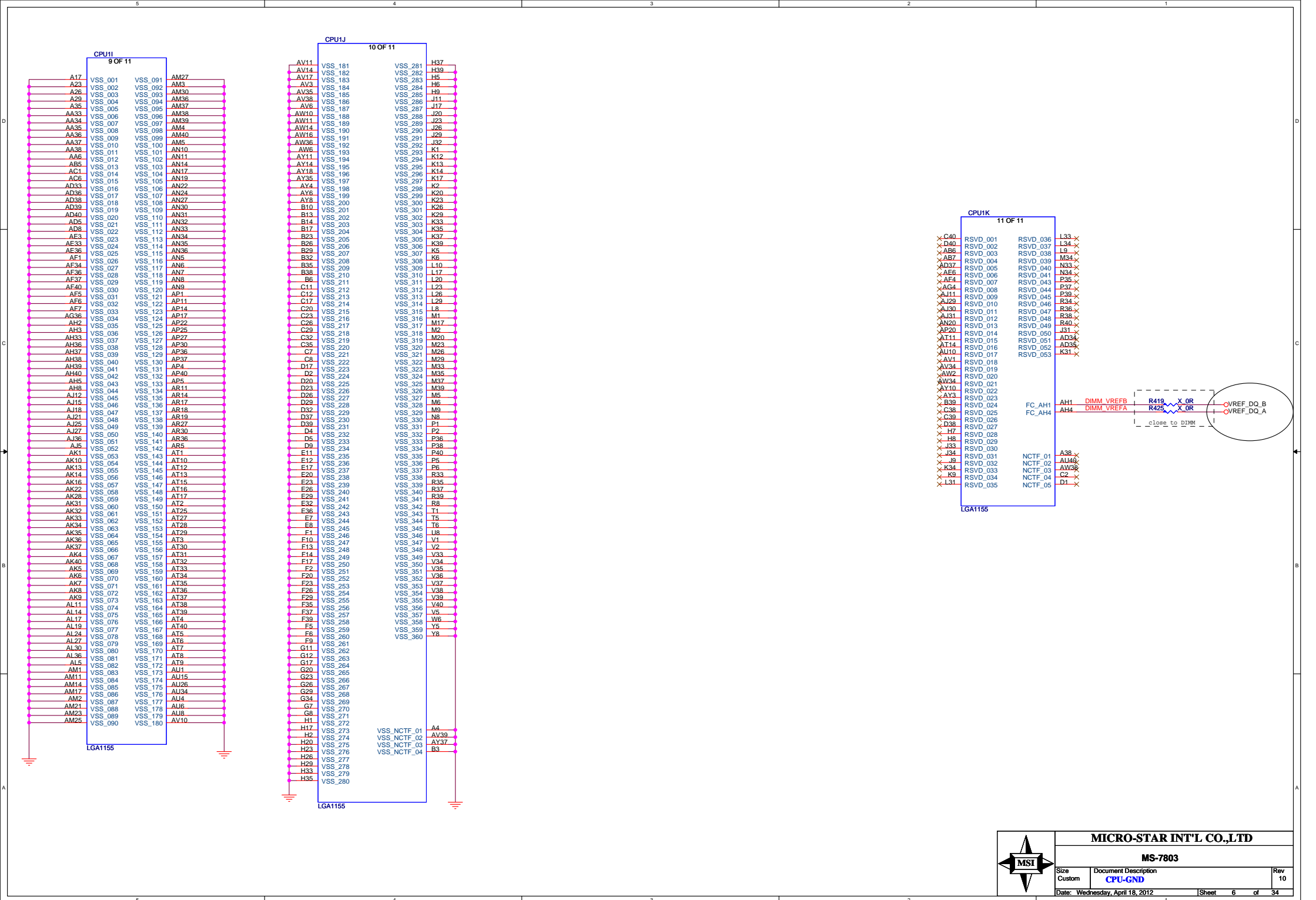
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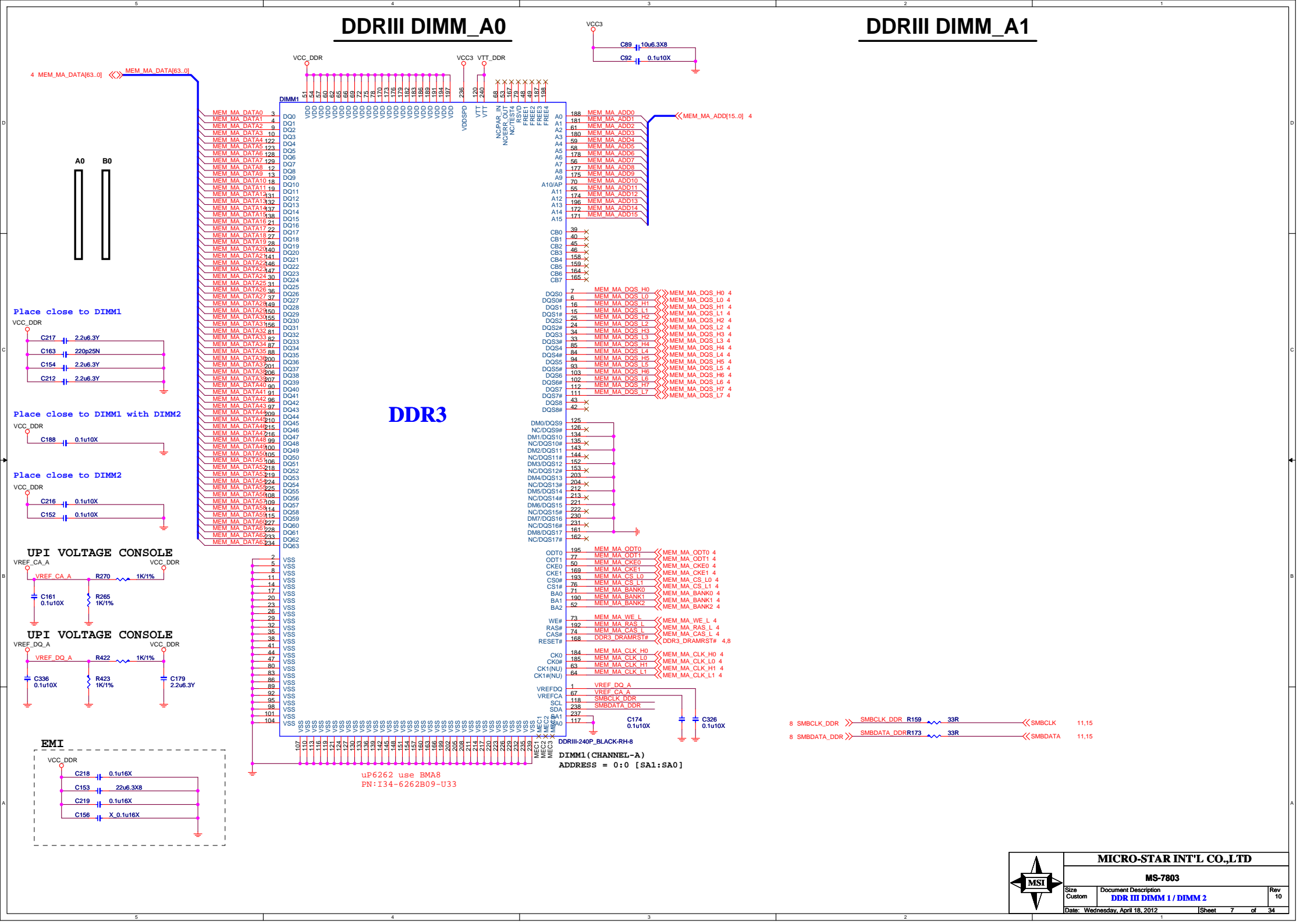






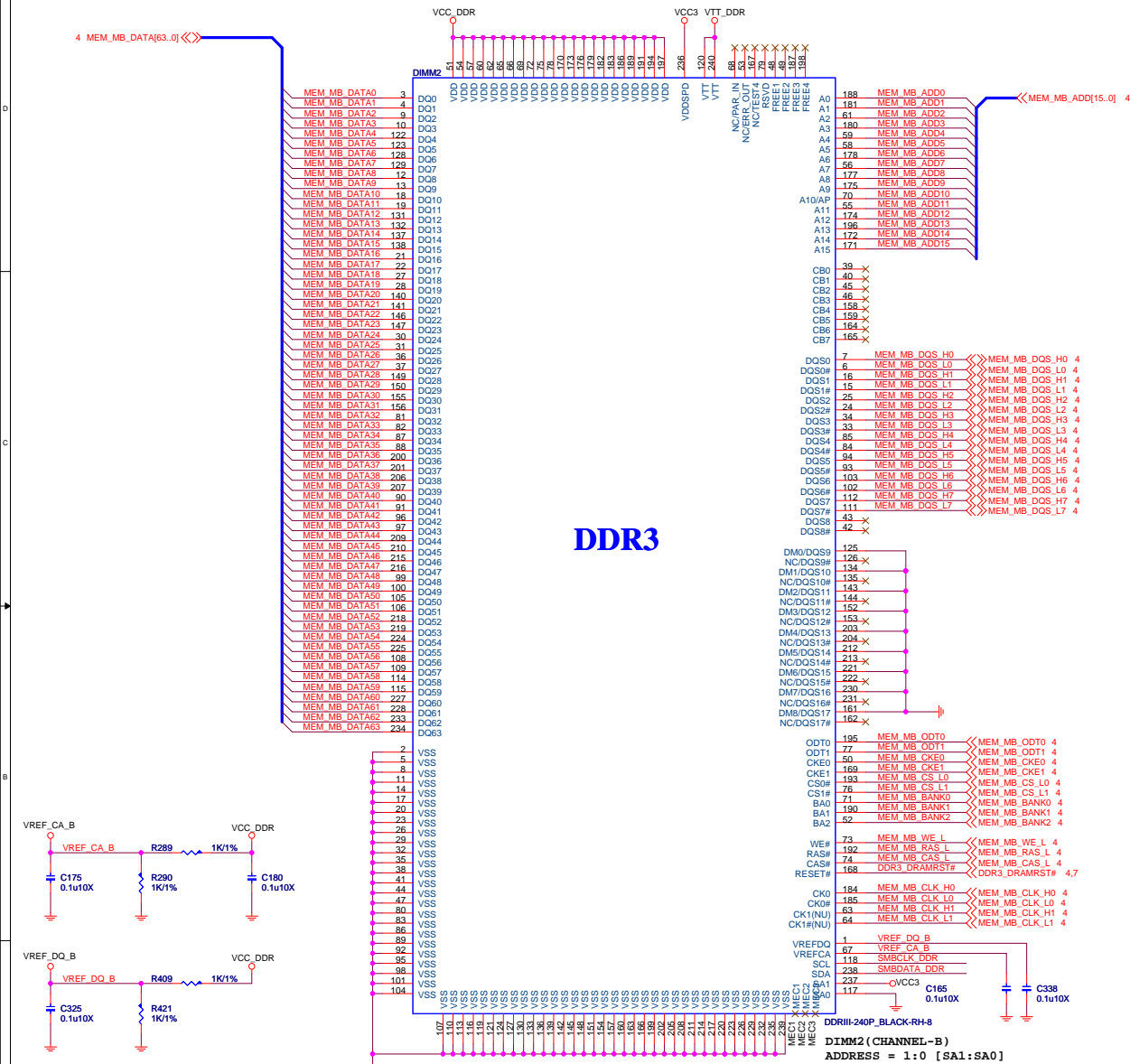
# DDRIII DIMM\_A0

# DDRIII DIMM\_A1

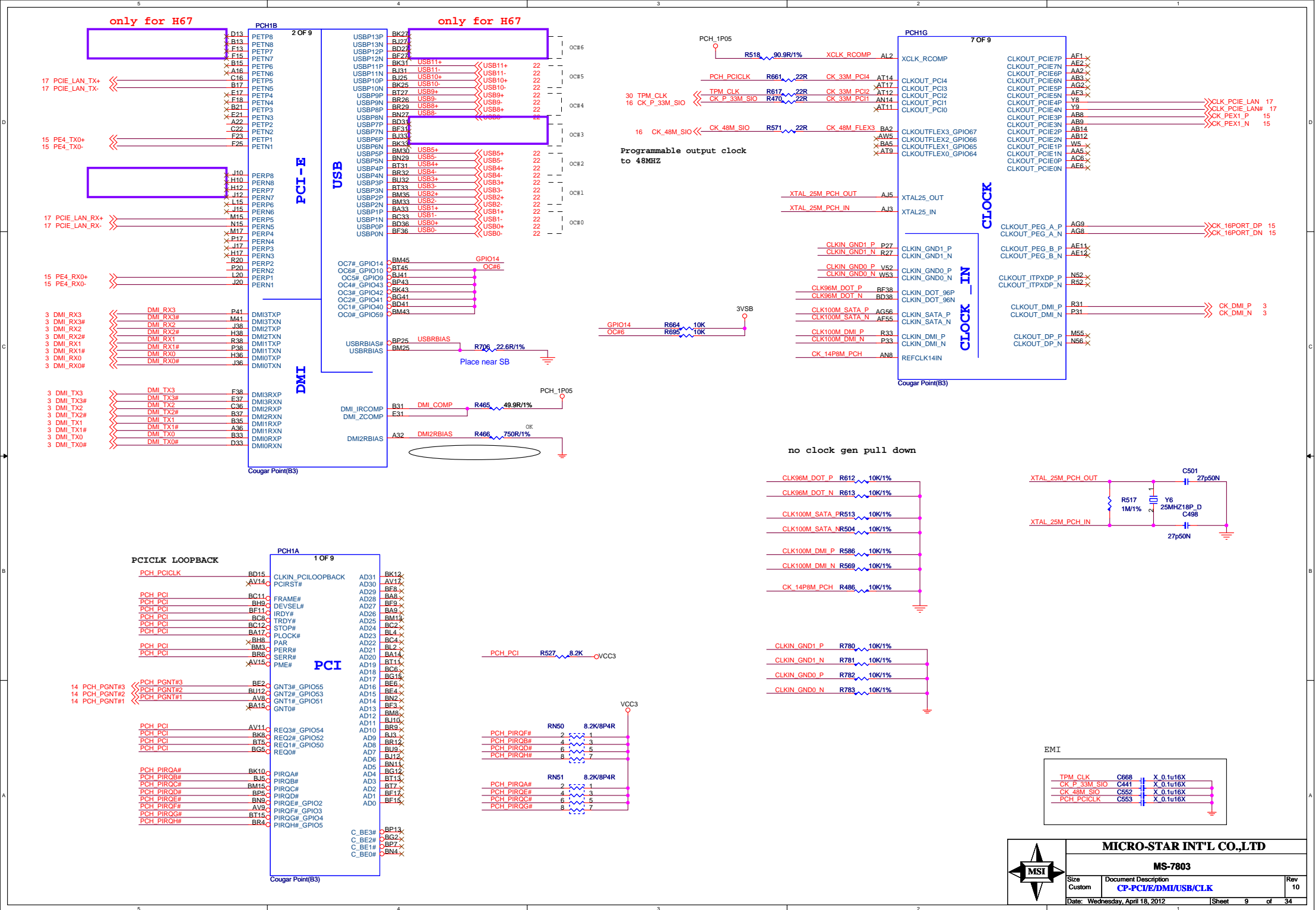


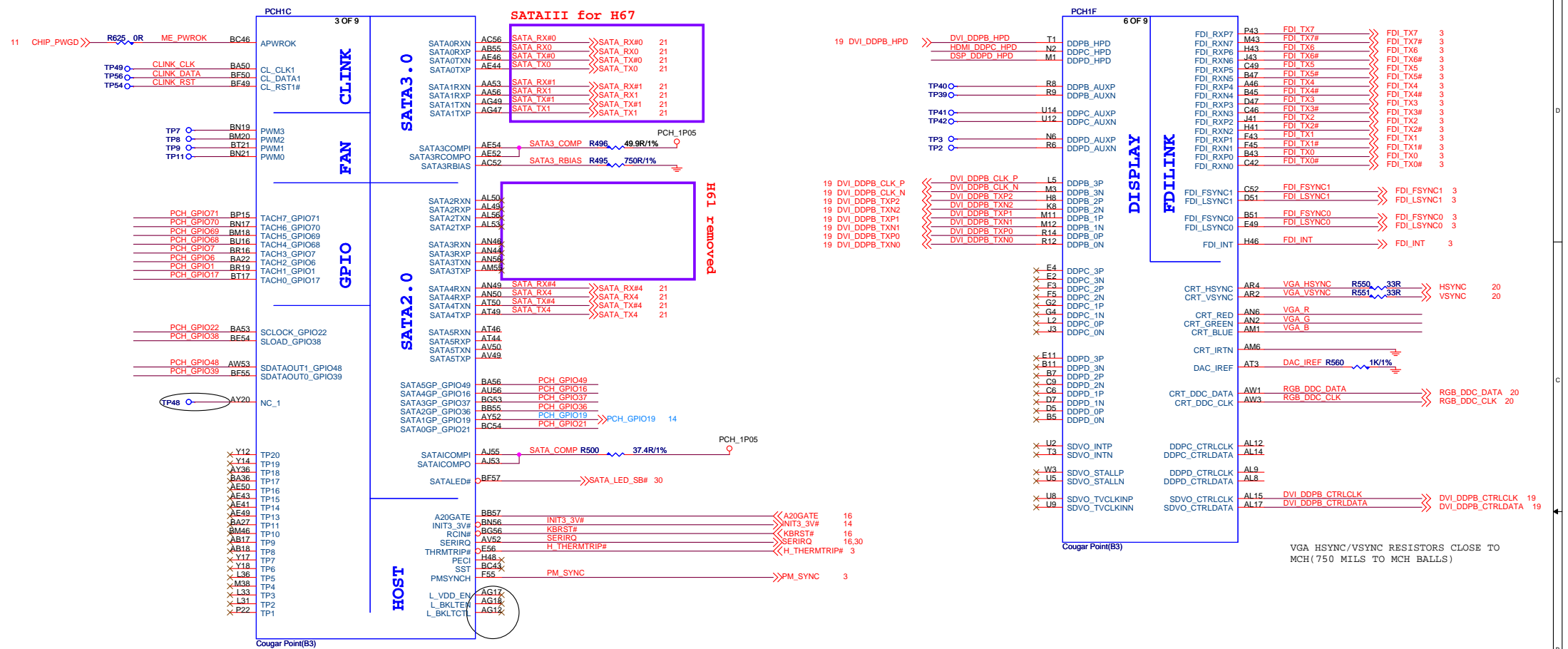


# DDRIII DIMM\_B0

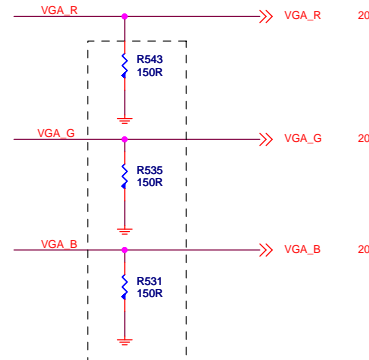
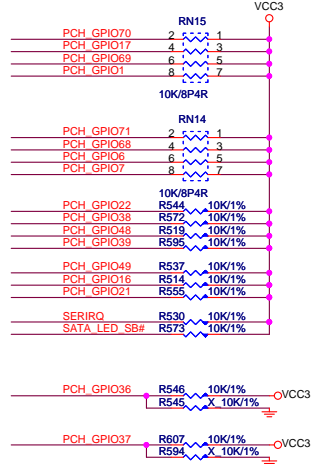




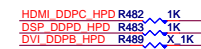




### Pull HIGH for PCH



No VGA( pull down)



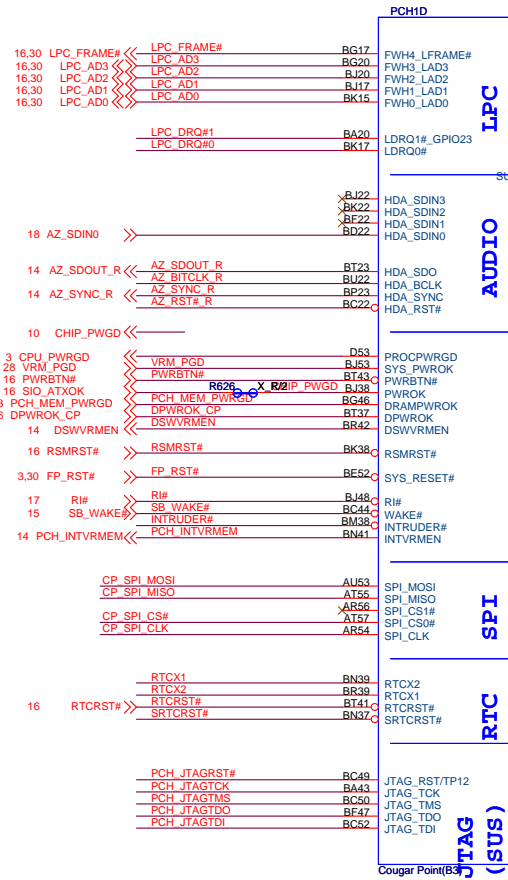
Enable VGA( CTRLCLK/DATA Pull High)



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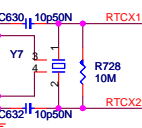
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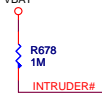


## RTC Block

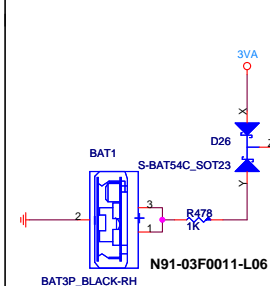
Close to PCH



## Chassis Intrusion

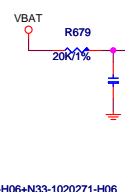


## RTC and CLR\_CMOS

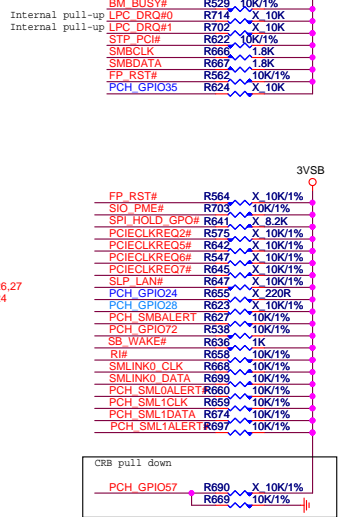


## Clear CMOS

CMOS CLEAR JUMPER	
JBAT1 Clear CMOS	
1 - 2 Normal	
2 - 3 Clear CMOS	

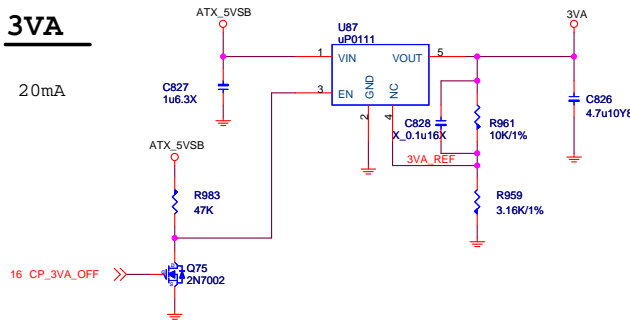


## REQUIRED STRAPS



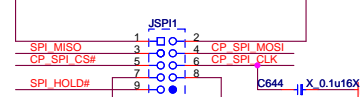
## 3VA

20mA



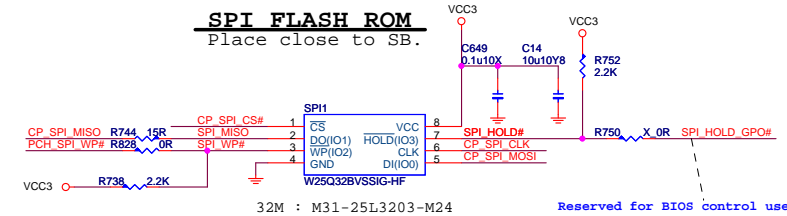
## SPI DEBUG PROT

Close to SPI ROM



## SPI FLASH ROM

Place close to SB.

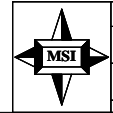
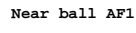
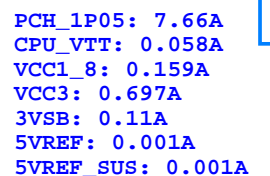


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Reserved for BIOS control used

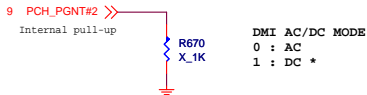
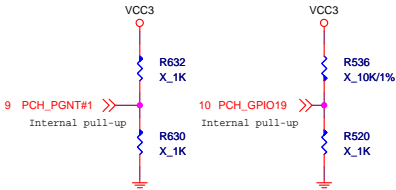


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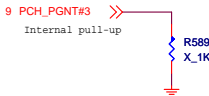


PCH Straps

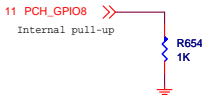
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



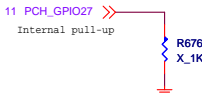
DMI AC/DC MODE  
0 : AC  
1 : DC \*



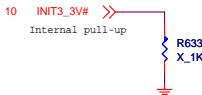
Topblock swap override when pull-low  
Signal has a weak internal pull-up



GPIO8  
0 : Integrated Clocking Enable (FCIM)\*  
1 : Buffer Through Mode Enable (BTM)

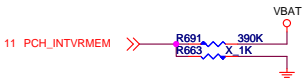


GPIO28  
0 : OD PLL VR disabled  
1 : OD PLL VR enabled \*  
Signal has a weak internal pull-up



INT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*

1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.



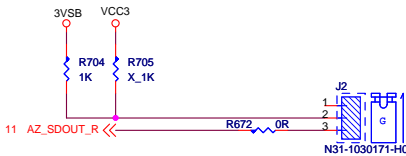
INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



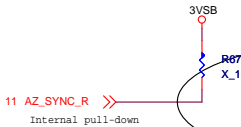
DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

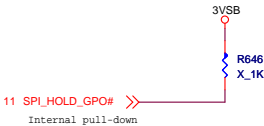


HDA\_SDO  
Disable ME in Manufacturing Mode  
when pull LOW ????

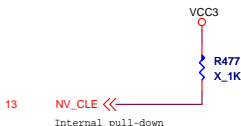
HDA\_SDO has internal pull down.  
Default should be connected to SDIN of codec, no pull up/down.  
To Disable ME need to have a jumper to pull high



HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY



GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



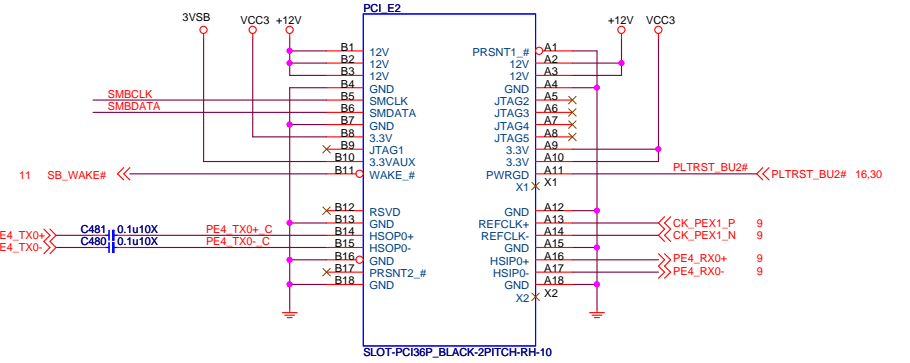
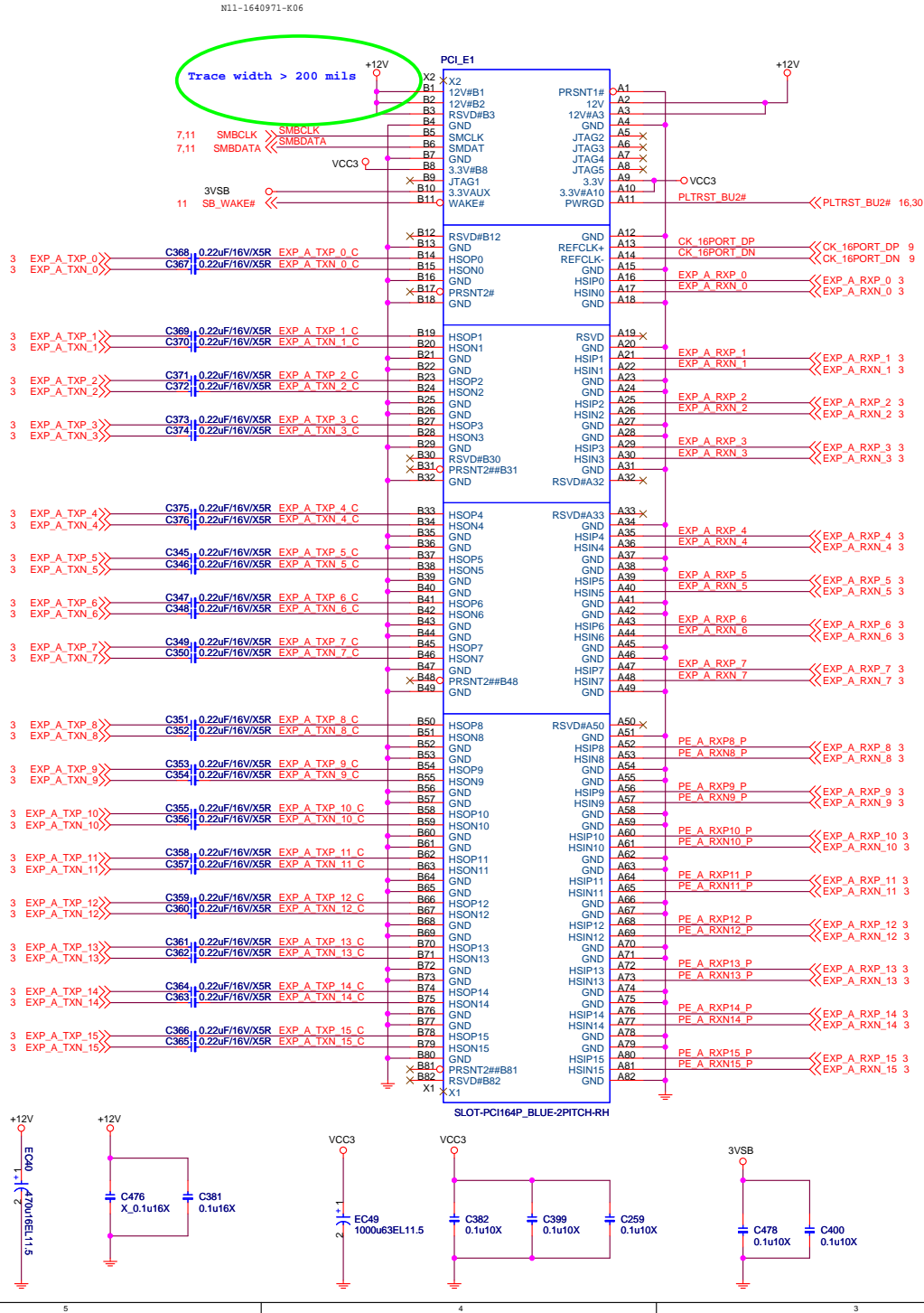
SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



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# PCI\_Express X16 Slot

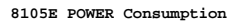
# PCI EXPRESS x1-PORT





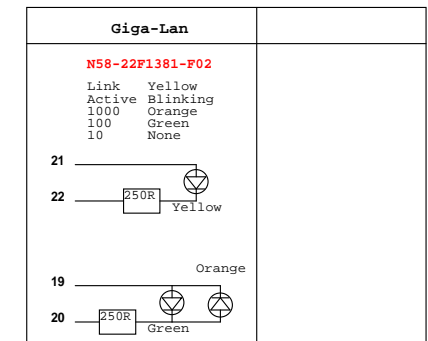
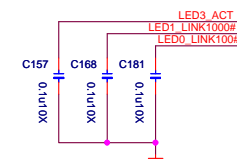


RTL8105E 10/100M LAN

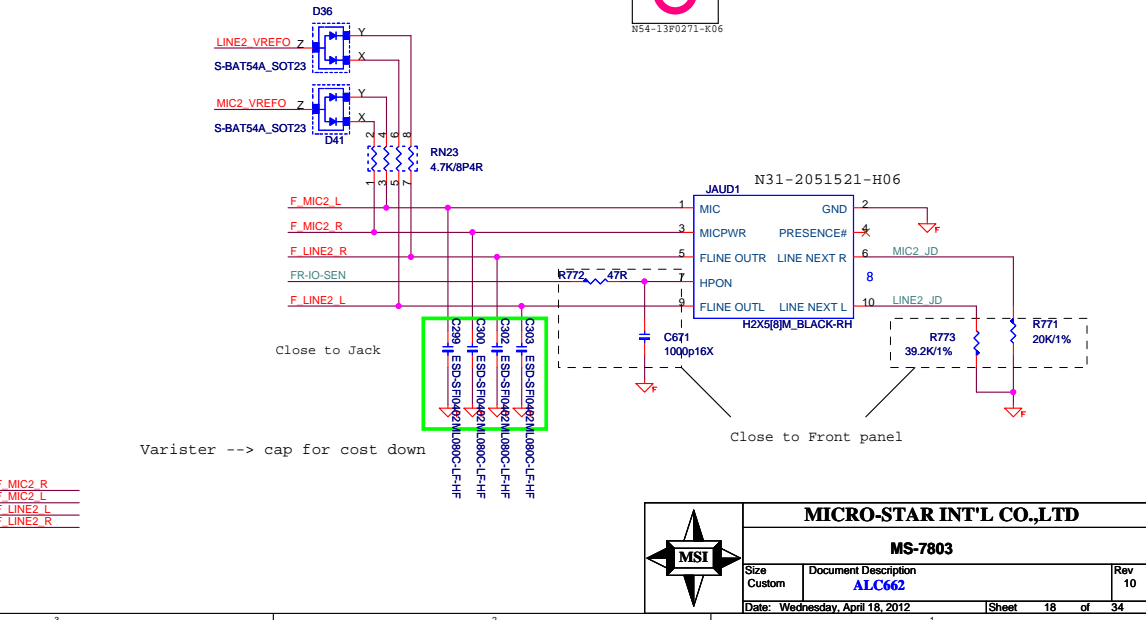
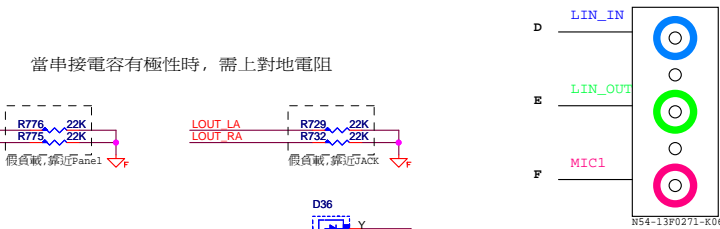
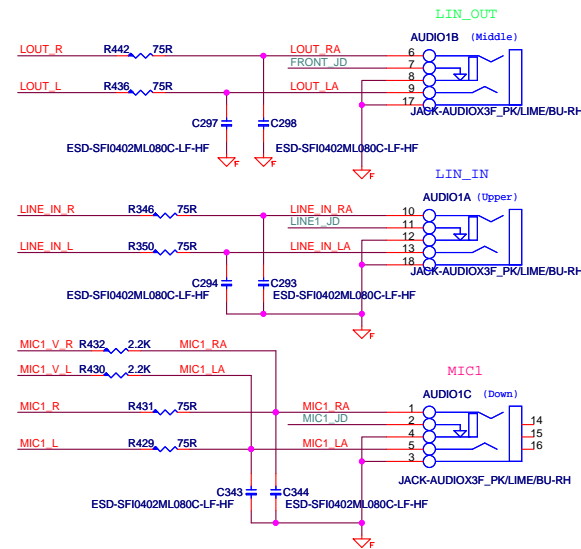
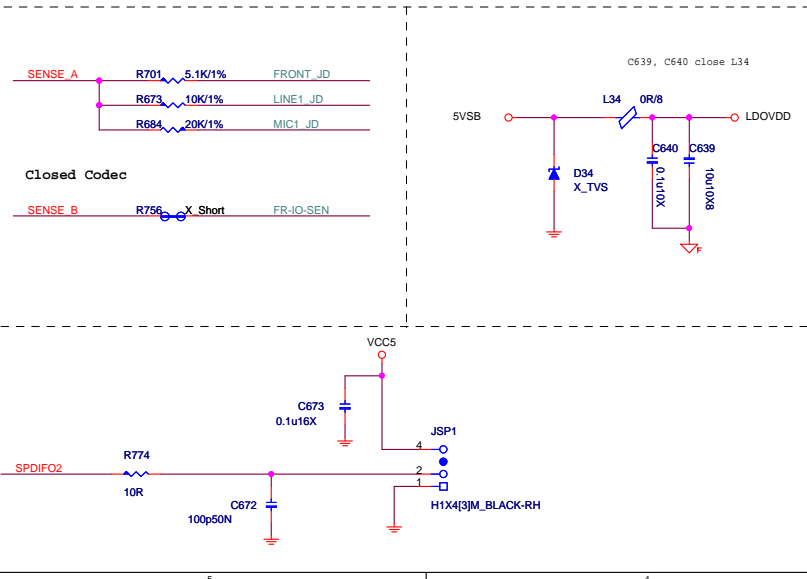
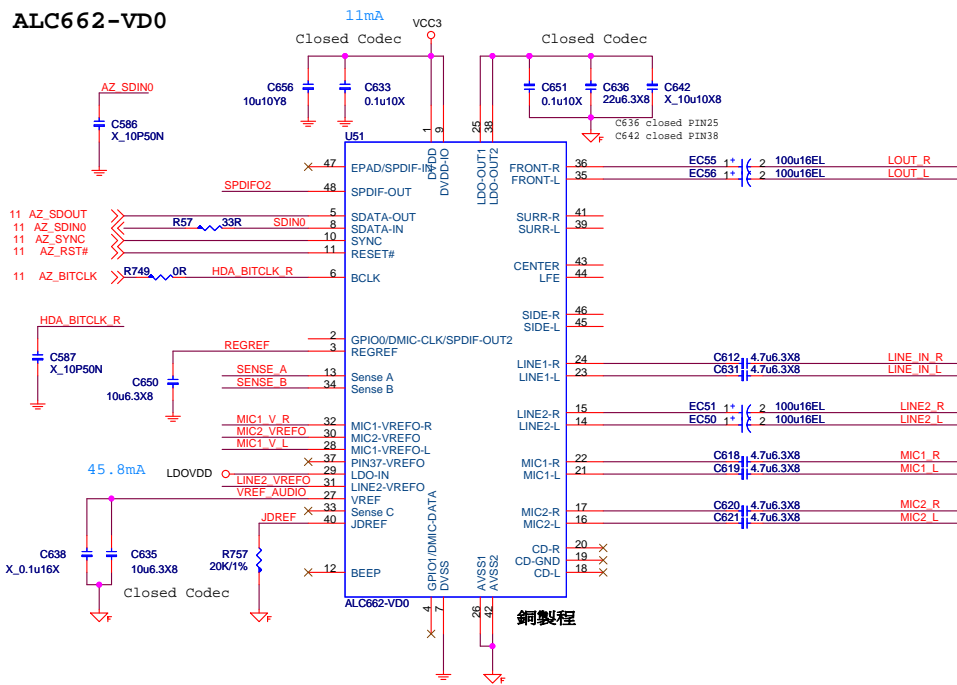


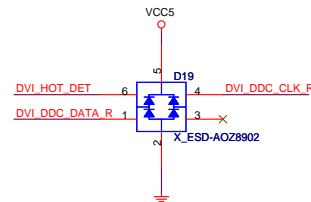
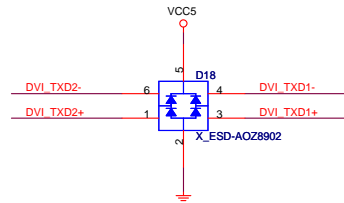
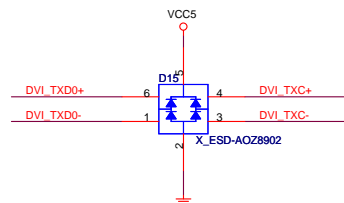
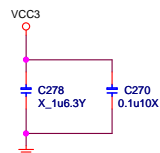
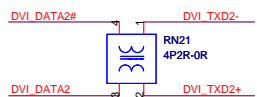
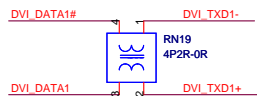
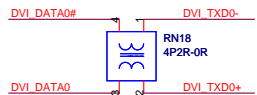
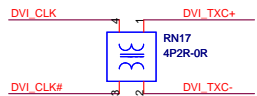
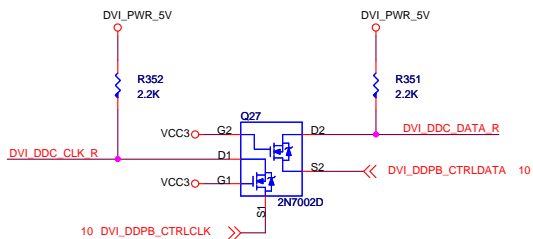
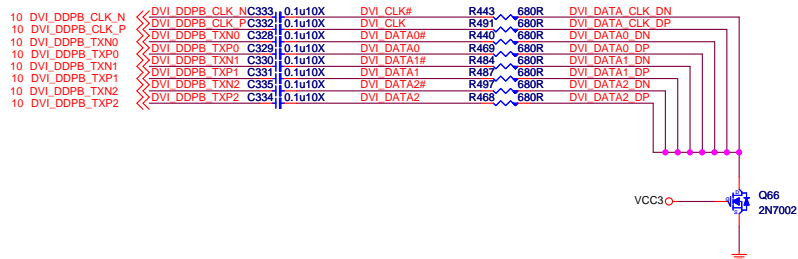
### 8111E POWER Consumption

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

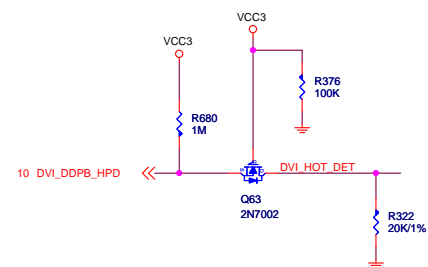
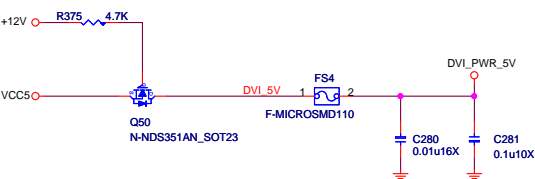
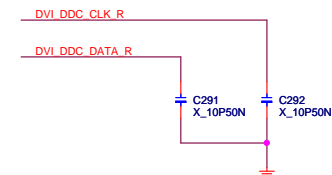
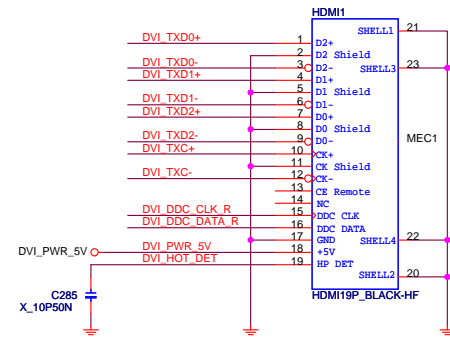
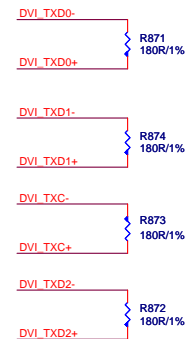


## ALC662-VD0





For EMI

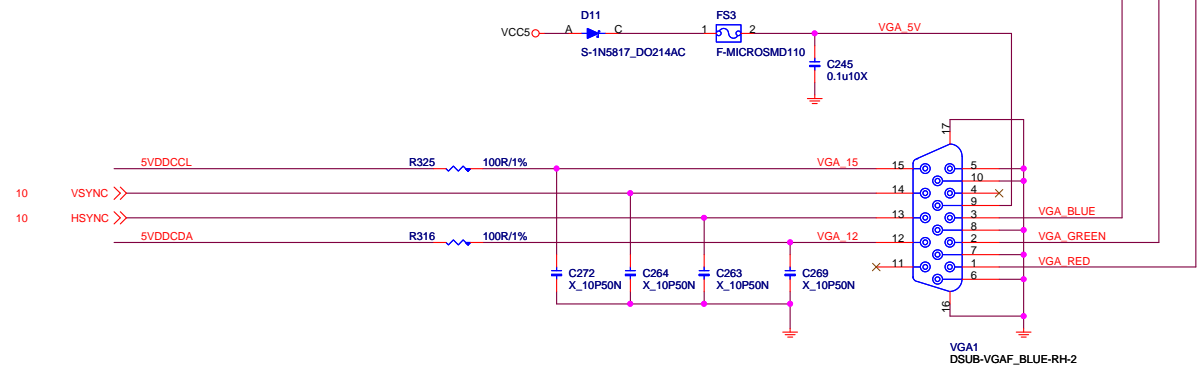
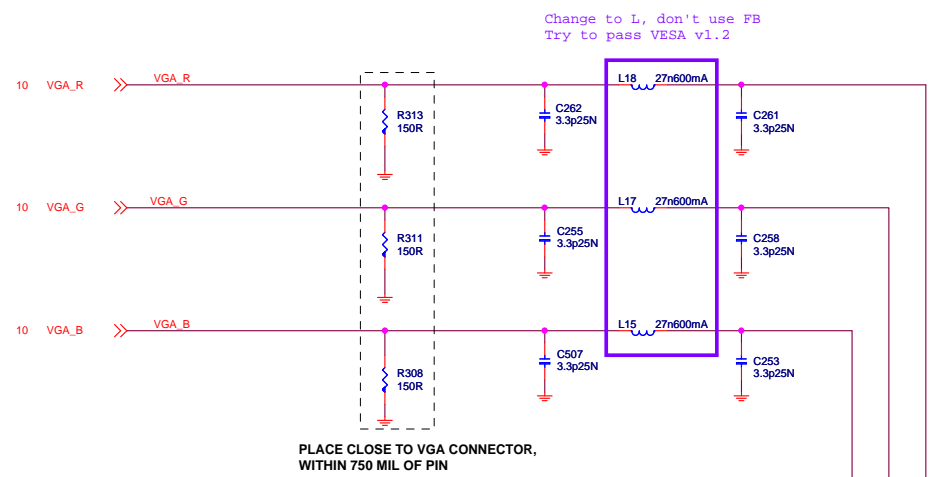
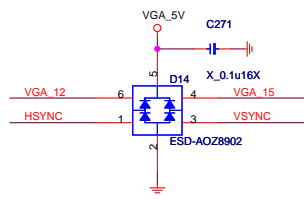
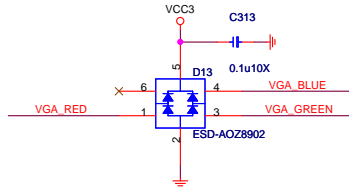
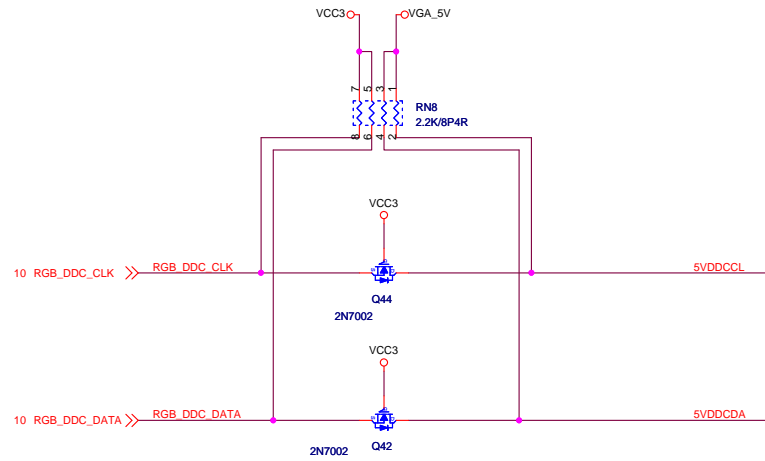


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D-Sub

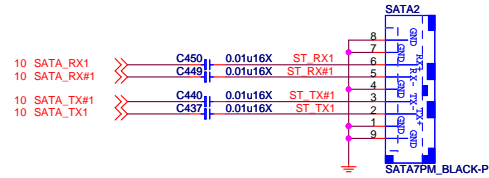
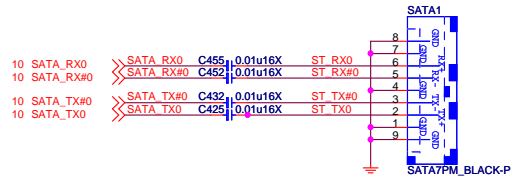
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



### SATA 6G PORT 0,1

H61 PORT 0/1 Support 3G  
H67 PORT 0/1 Support 6G

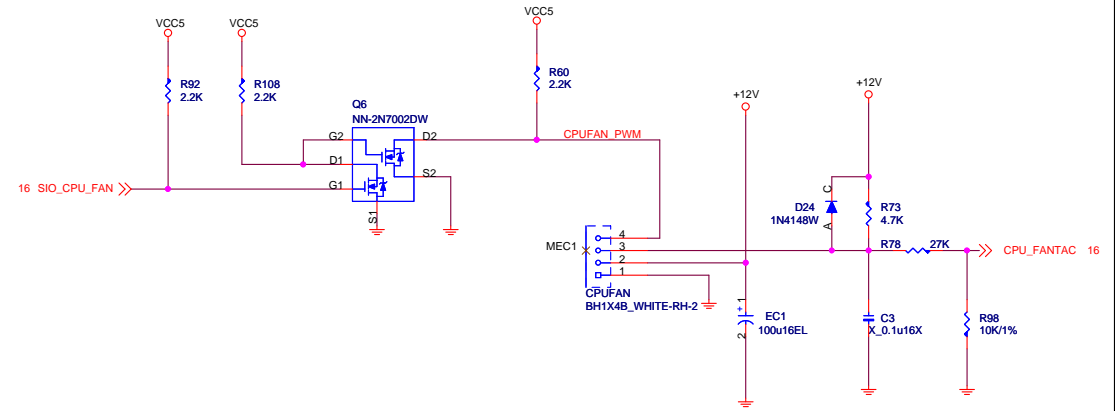


### SATA 3G PORT 2,3

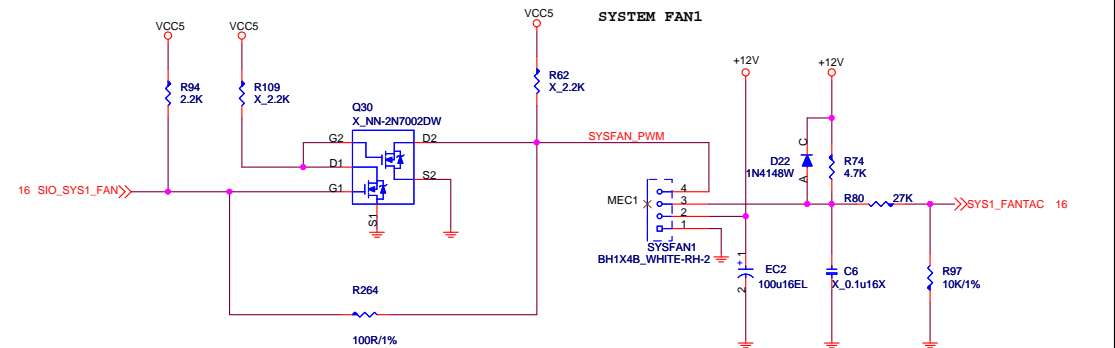
For H61, SATA2&3 removed



### CPU FAN-COUNTROL CIRCUIT



### SYSTEM FAN-COUNTROL CIRCUIT

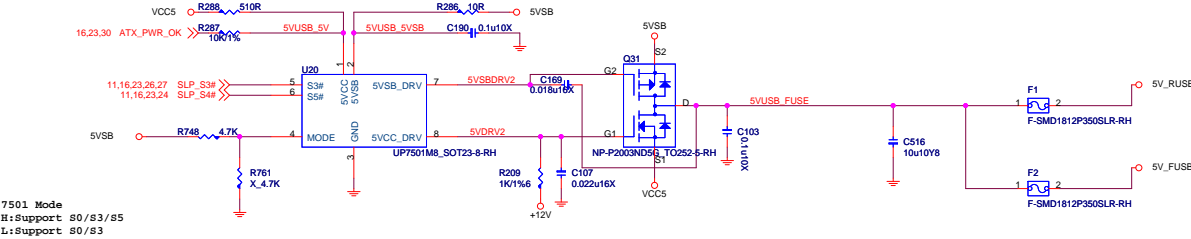


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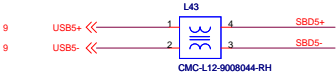
5V\_RUSB Switch



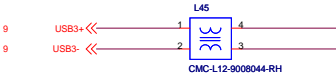
Front USB Connector

For H61 6,7,12,13 Port should be remove

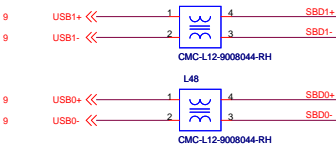
FRONT USB PORT 4,5



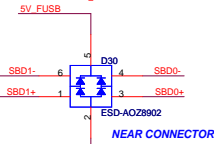
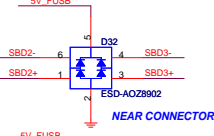
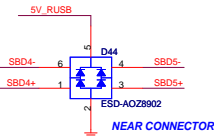
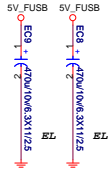
FRONT USB PORT 2,3



FRONT USB PORT 0,1

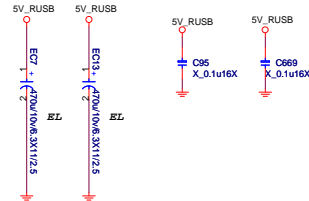


NEAR USB Front CONNECTOR

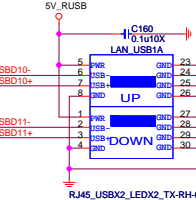
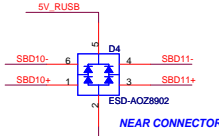
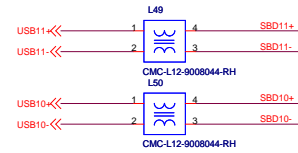


Rear USB Connector

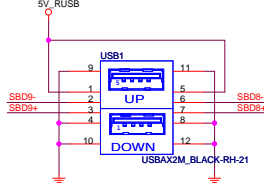
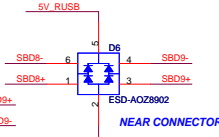
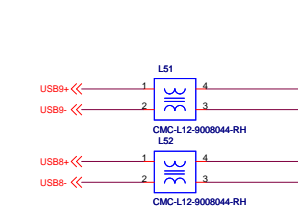
NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)

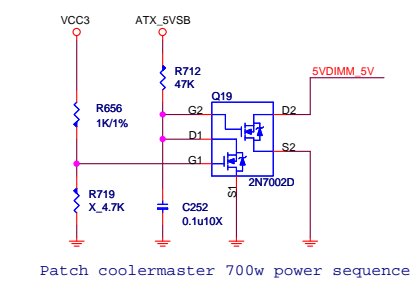
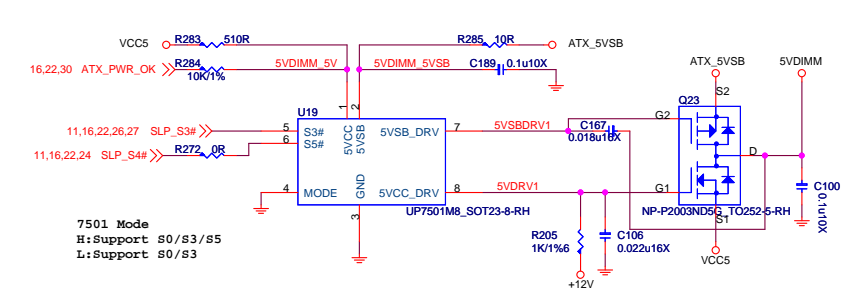


REAR USB PORT 8,9 (With PS2)



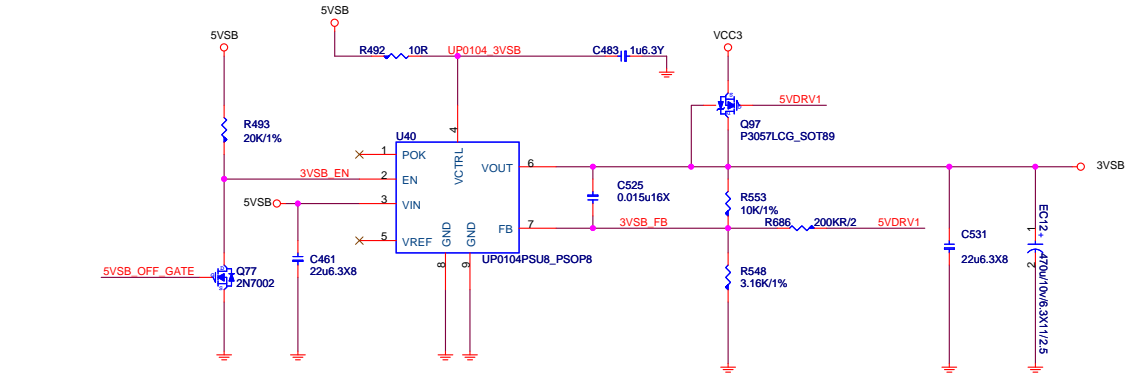


5VDIMM FOR DDR

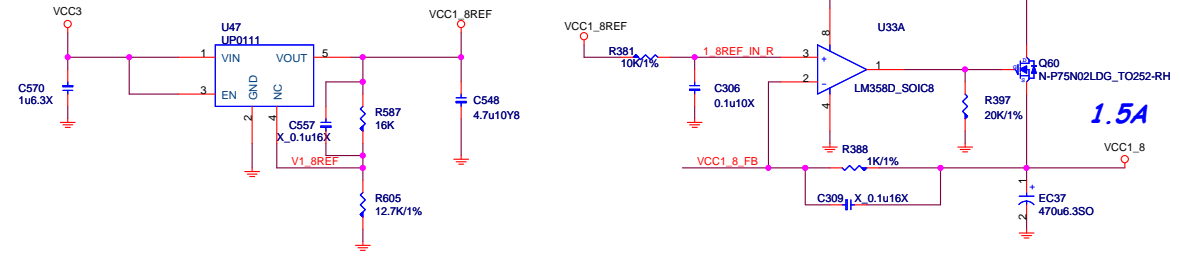


3VSB

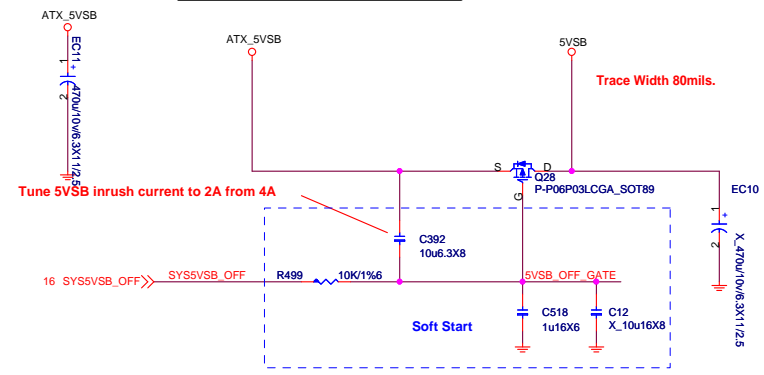
3VSB supply to PCH and other device.  
Turn off when Deep S3/S5 by 5VSB off.



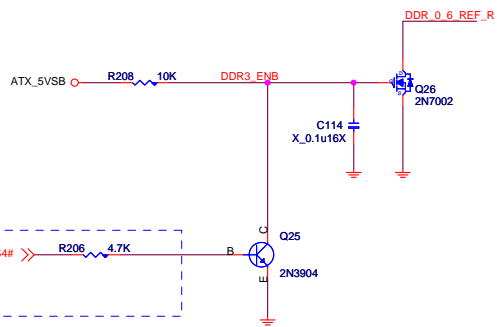
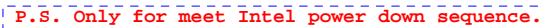
VCC1\_8REF



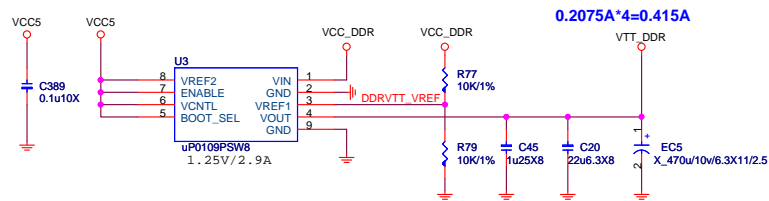
5VSB Power Switch



4.5A FOR CPU  
7.5A FOR 2DIMM  
1A FOR DDR VTT



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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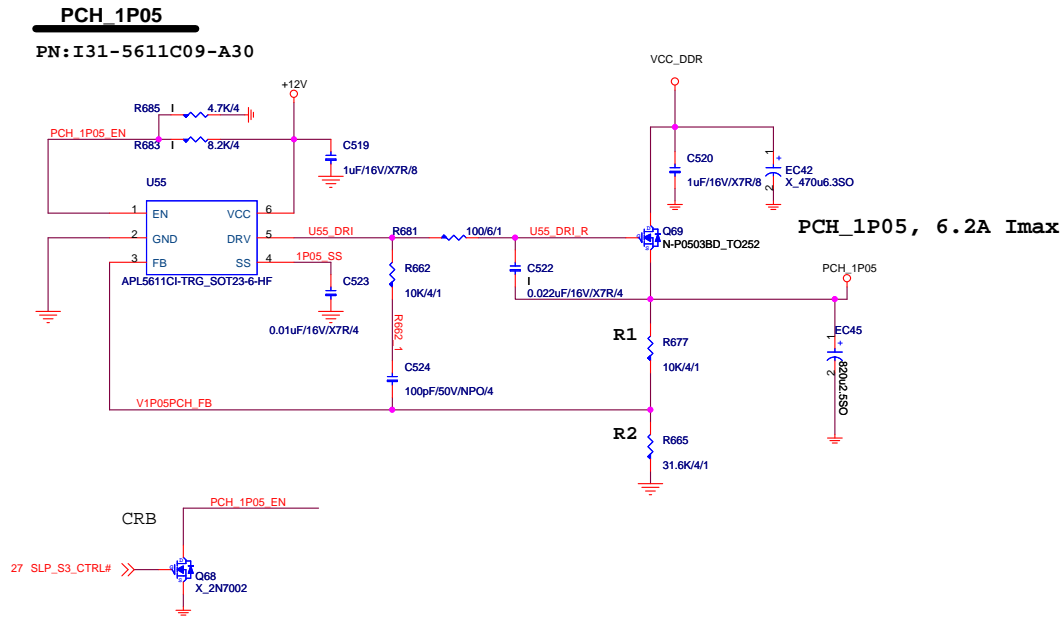
Size Custom	Document Description <b>DDR Power - uP1513 1-Phase</b>	Rev 10
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# PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE

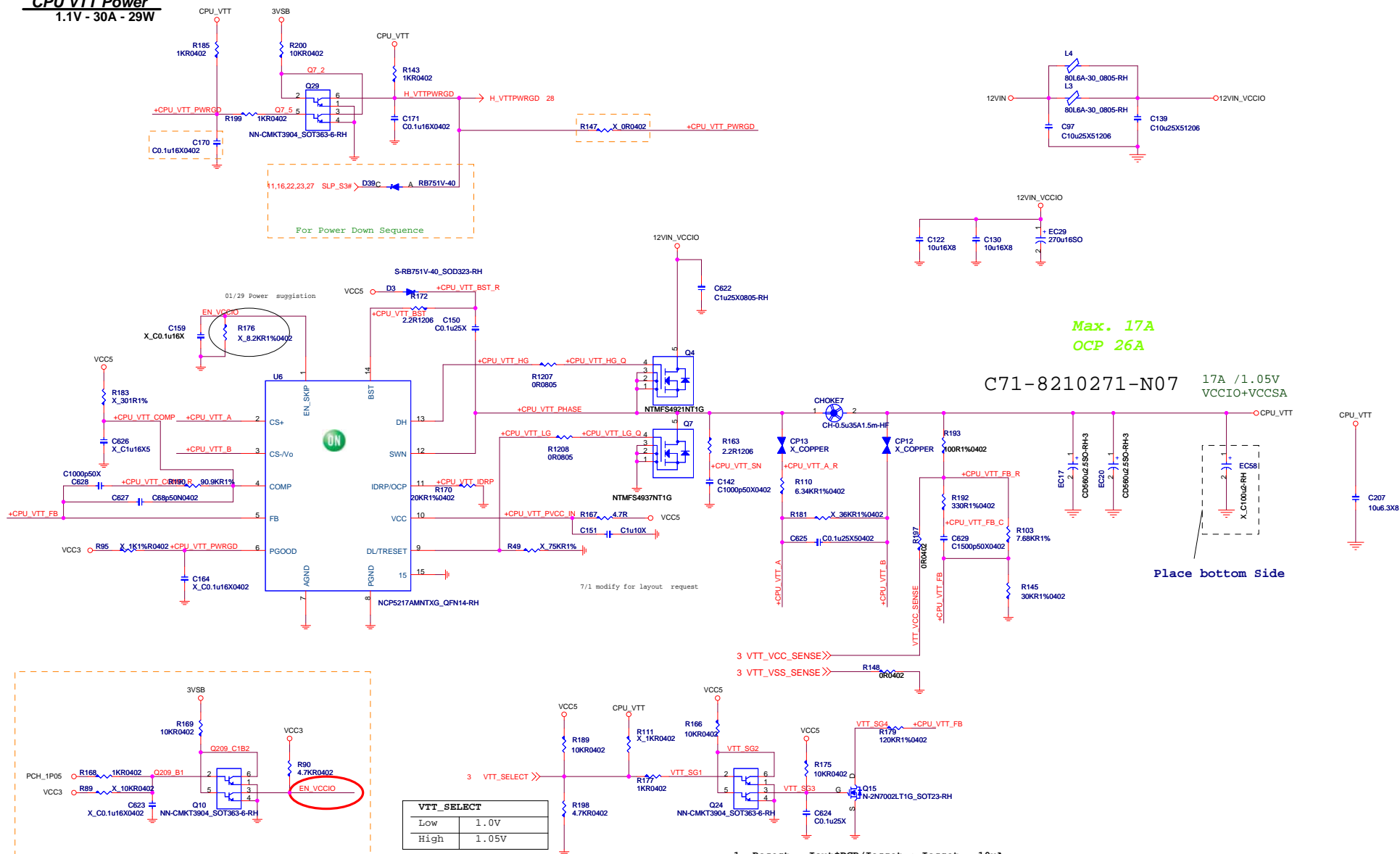


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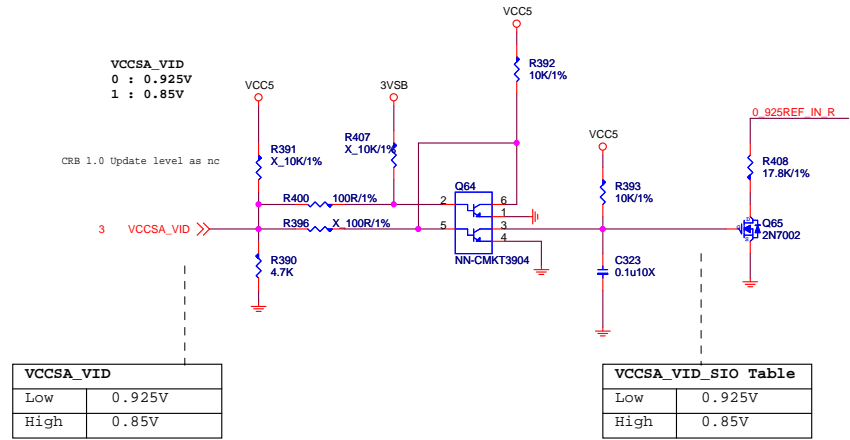
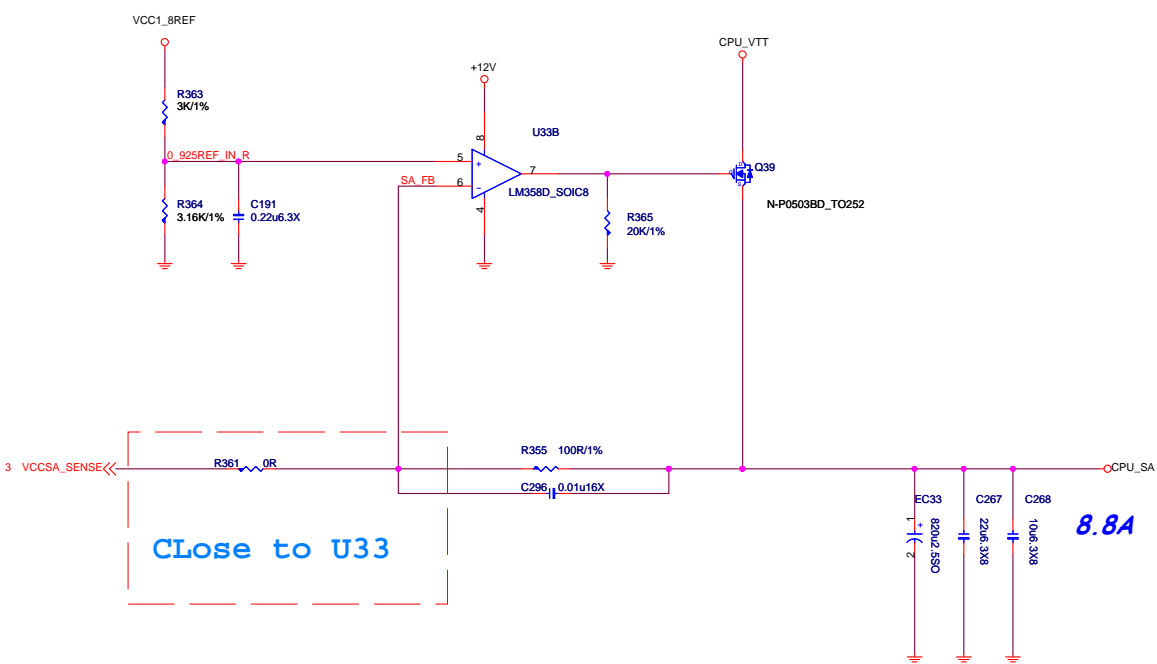
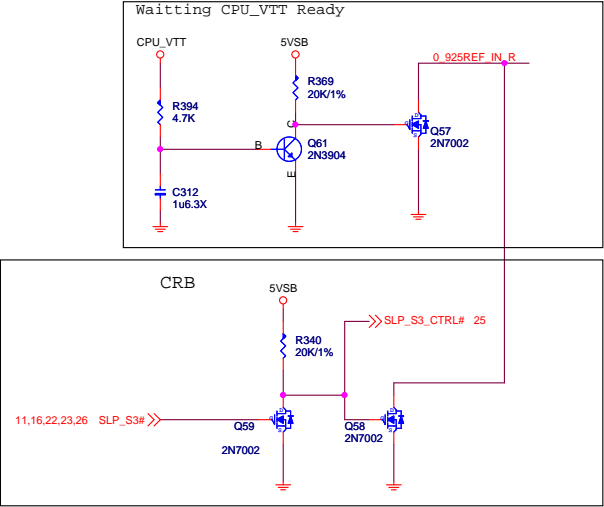
**CPU VTT Power**  
1.1V - 30A - 29W



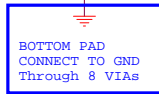
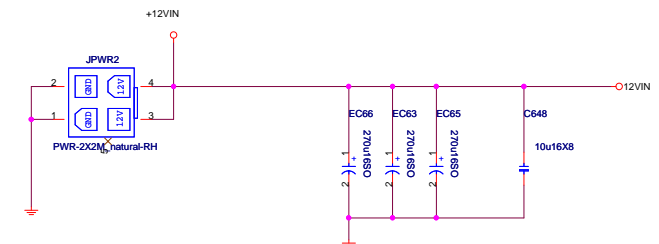
1.  $R_{ocset} = I_{out} \cdot DCR / I_{ocset}$  ;  $I_{ocset} = 10\mu A$   
If  $DCR = 1m$  ;  $I_{out} = 20A$ ,  $R_{ocset} = 20A \cdot 1m / 10\mu A \rightarrow R_{ocset} = 2K$
2.  $C_{sen} = L / R_{ocset} \cdot DCR$   
If  $DCR = 1m$  ;  $L = 1\mu$ ,  $C_{sen} = 1\mu / 2K \cdot 1m \rightarrow C_{sen} = 0.5\mu$

CPU\_SA:0.925/0.85

SA Core =8.8A



## VRM 12V Input

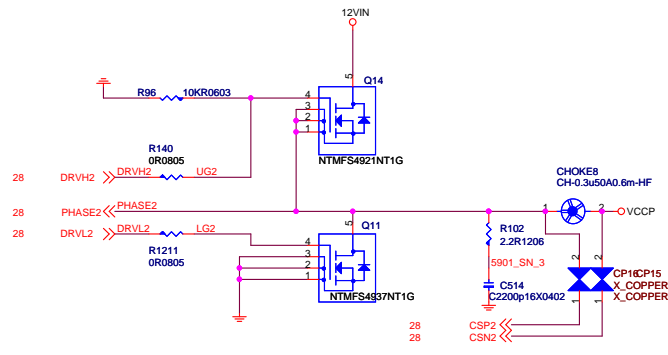
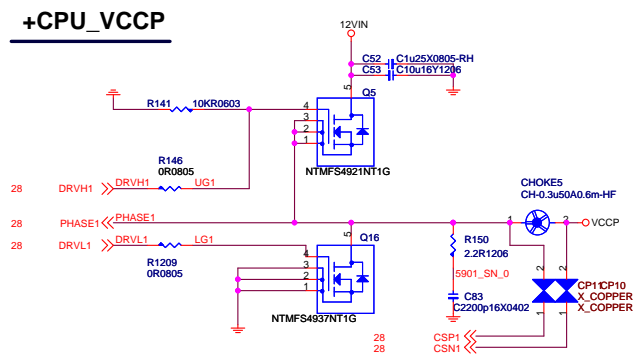


BOTTOM PAD  
CONNECT TO GND  
Through 8 VIAs

ERT-J0EV474J  
CLOSE Q1

ERT-J0EV474J  
CLOSE Q5

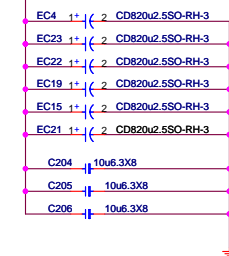
## +CPU\_VCCP



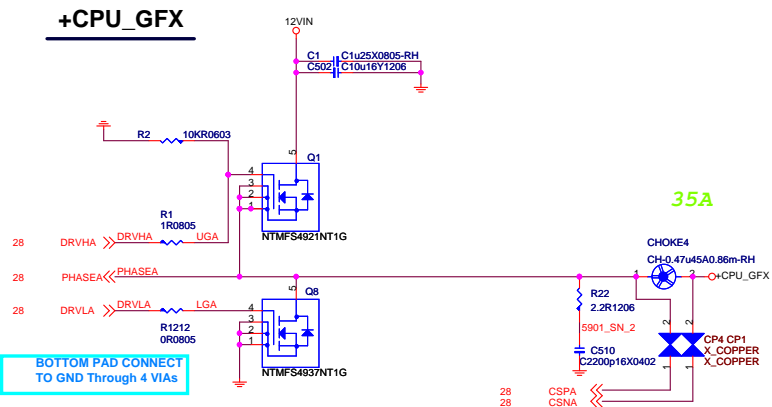
Max.85A  
OCP 1.12A

## +CPU\_VCCP Output Caps

C71-8210271-N07



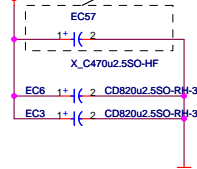
## +CPU\_GFX



35A

C71-8210271-N07

+CPU\_GFX Place bottom Side



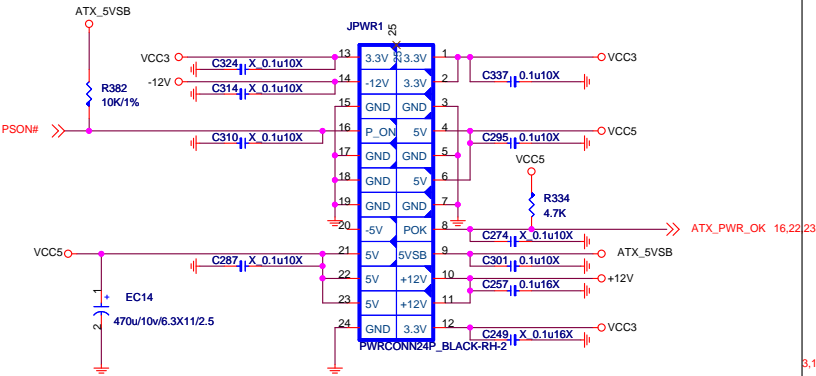
BOTTOM PAD CONNECT  
TO GND Through 4 VIAs



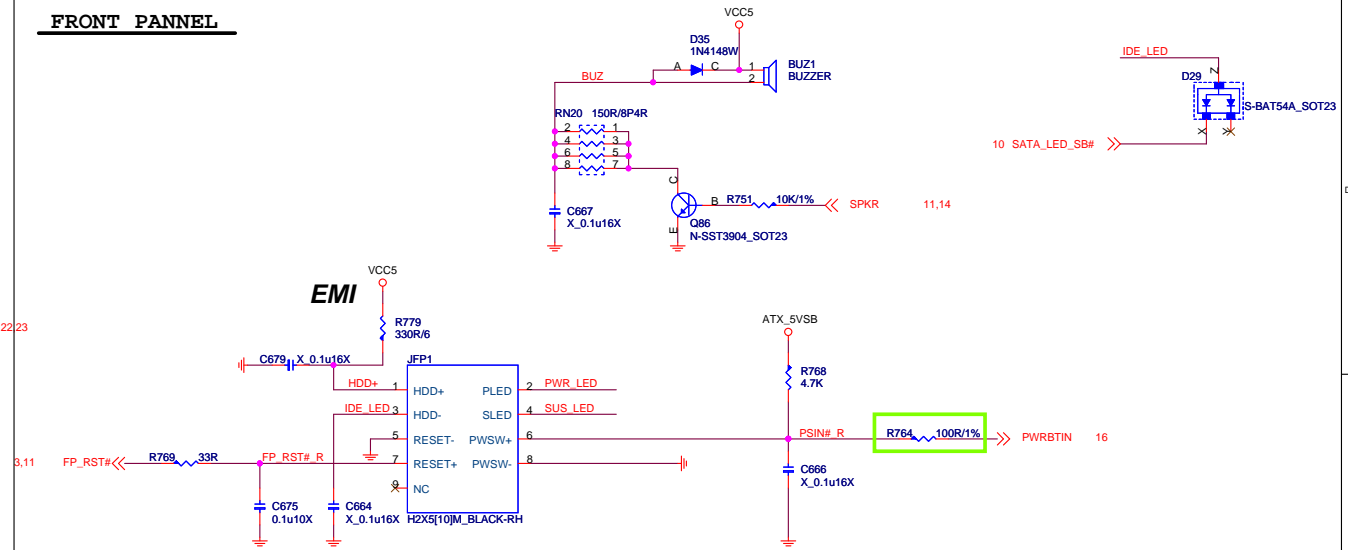
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MS-7803			
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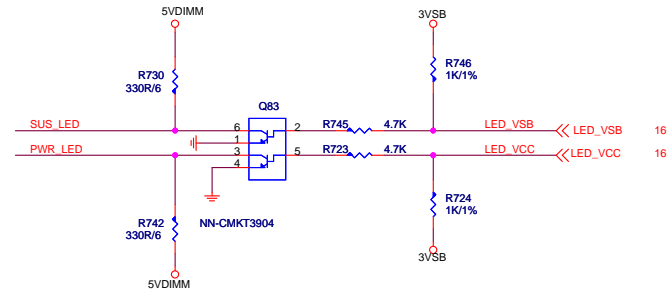
### ATX POWER CONNECTOR



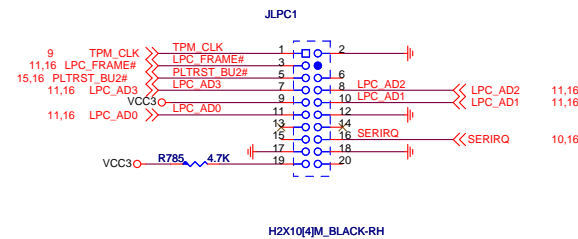
FRONT PANNEL



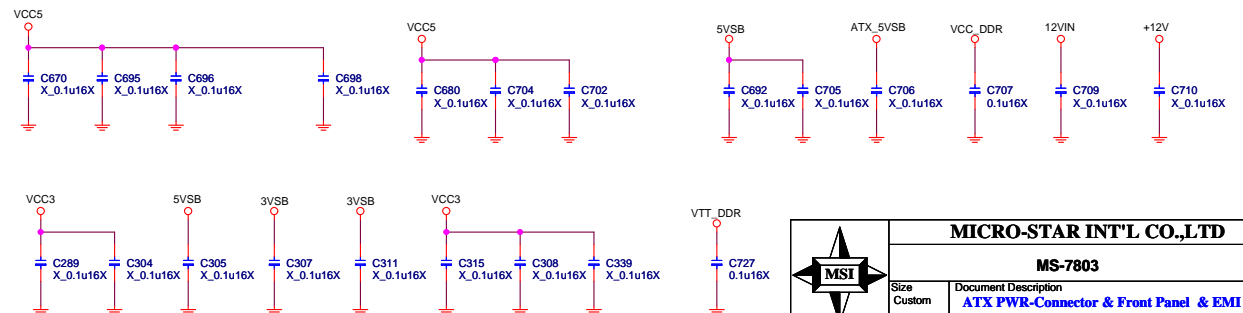
LED ( for Fintek 71869)



***JLPC***



## EMI

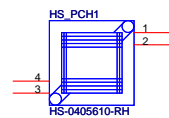


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PCH XDP PWRGD/RESET



7803-10



BAT-BCR2032P-RH



X\_Rubber



X\_Rubber

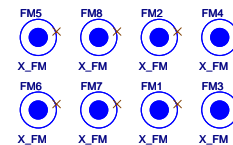


E21-7557050-L06

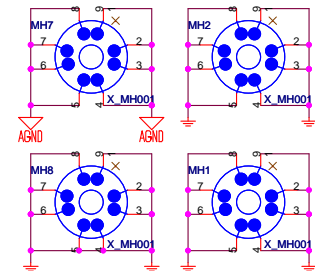
Simulation



Optical Fiducial Marks-120



Mounting Holes



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Custom	XDP / Manual Parts	10
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